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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRAN, MICHAEL THANH	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,188	LINDE ET AL.	
	Examiner	Art Unit	
	Michael t. Tran	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-26 and 28-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-19* is/are allowed.

6)☒ Claim(s) *1-4,6,11-13,20,24-26 and 31* is/are rejected.

7)☒ Claim(s) *4,7-10,21-23,29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MICHAEL TRAN
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated February 16, 2006, claims 1-4, 6-26 and 28-31 are active in this application.

Claim Objections

2. Claims 4, 7-10, 21-23, 29 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections – 35 U.S.C. § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 1-3, 6 and 11-13 stand rejected under 35 U.S.C 102(e) as being anticipated by Pekny [U.S. Patent #6,553,510].

With respect to claim 1, Pekny discloses a method comprising: detecting [via a erase or program operation – se column 2] an electrical characteristic identifying a defect in a memory unit [302 of figure 3]; and replacing the memory unit with an alternate memory unit [304 of figure 3], wherein the replacing is performed during user operation [erase or program – see figures 4 and 5] of a device having the memory unit and the alternate memory unit; wherein the detecting is performed during an erase operation. See columns 1 and 2. In the cited columns, Pekny discloses that if particular memory is identified to be defective, it is replaced with alternate memory [redundant memory] during the erase and programming operation of the memory.

With respect to claim 2, Pekny discloses, in figure 4, that the detecting the electrical characteristic comprises: monitoring a current [pulses] during an erase attempt [via 410]; and identifying the defect when the current [pulses] passes a predetermined current threshold [via 410, 414, 416 and 420]. It is noted that Pekny disclose that a particular cell is detected to be defective by way of the application of erase pulses with a predetermined maximum times [threshold]. Additionally, it is noted that the pulses are voltage pulses that are a function of current times the resistance. Further, a change in voltage would yield a change in current and resistance. Furthermore, Pekny discloses, in columns 1 and 2, that the detection of a defective memory is done during an erase and programming operation. Also see figures 4 and 5.

With respect to claim 3, Pekny discloses, in figure 4, that the detecting the electrical characteristic comprises: monitoring a voltage [pulses] during an erase attempt [via 410]; and identifying the defect when the voltage [pulses] passes a predetermined voltage threshold [via 410, 414, 416 and 420]. It is noted that Pekny disclose that a particular cell is detected to be defective by way of the application of erase pulses with a predetermined maximum times [threshold].

With respect to claim 6, Pekny discloses, in column 6, that the replacing memory unit with the alternate memory unit comprises: causing the memory unit to be un-accessible at a memory address [defective cell]; and causing the alternate memory unit to be accessible at the memory address [redundant cell]. It the cited section, Pekny indicated that "...access the redundant memory cells in response to address locations of defective primary cells locations..." Further, Pekny discloses that once the defective memory is detected, its accessibility is routed to the replacement memory, thereby rendering the defective memory inaccessible.

With respect to claim 11, Pekny discloses that the memory is a flash memory. See column 1.

With respect to claim 12, Pekny discloses that the memory is a flash memory. It is known that the memory is arranged in rows and columns. See column 1.

With respect to claim 13, Pekny discloses that he memory is a polymer. See column 1.

5. Claim 20 is rejected under 35 U.S.C 102(e) as being anticipated by

Santin [U.S. Patent #6,847,574].

With respect to claim 20, Santin discloses, in figures 1, 2 and 5, a processor [506]; an antenna [504] coupled to the processor [indirectly]; and a memory device [508 – flash memory] coupled to the processor, the memory device comprising: a plurality of accessible memory units [110 of flash memory 100 of figure 1]; one or more redundant memory units [108]; a failure detection unit [108 – see column 1, lines 25-40] coupled to the plurality of accessible memory units configured to monitor electrical characteristics in the plurality of accessible memory units and to detect an electrical characteristic that identifies a defect in one of the plurality of accessible memory units; and a redundant block swap unit [206] coupled to the accessible memory units and the one or more redundant memory units, the redundant block swap unit configured to replace the one of the plurality of accessible memory units with one or more redundant memory units.

6. Claims 24-26, 28 and 31 are rejected under 35 U.S.C 102(e) as being anticipated by Pekny [U.S. Patent #6,553,501].

With respect to claim 24, Pekny discloses, in figures 1-5, an apparatus comprising: a computer readable medium [eeprom or 140]; and instructions [logic] stored on the computer readable medium [see columns 1 and 2] to: detect [via a erase or program operation – see column 2] an electrical characteristic that identifies a defect in a memory unit [302 of figure 3]; and replace the memory unit with an alternate memory unit [304 of figure 3], wherein replacing is performed during user operation [erase or program – see figures 4 and 5] of a device having the memory unit and the

alternate memory unit. See columns 1 and 2. In the cited columns, Pekny discloses that if particular memory is identified to be defective, it is replaced with alternate memory [redundant memory] during the erase and programming operation of the memory.

With respect to claim 25, Pekny discloses that the instructions to detect the electrical characteristic comprises instructions to: monitoring a current; and identify the defect when the current [pulses] passes a predetermined current threshold [via 410, 414, 416 and 420]. It is noted that Pekny disclose that a particular cell is detected to be defective by way of the application of erase pulses with a predetermined maximum times [threshold]. Further, it is noted that the pulses are voltage pulses that are a function of current times the resistance. Furthermore, a change in voltage would yield a change in current and resistance.

With respect to claim 26, Pekny discloses, in figure 4, that the instructions to detect the electrical characteristic comprises instructions to: monitor a voltage [pulses] during an erase attempt [via 410]; and identify the defect when the voltage [pulses] passes a predetermined voltage threshold [via 410, 414, 416 and 420]. It is noted that Pekny disclose that a particular cell is detected to be defective by way of the application of erase pulses with a predetermined maximum times [threshold].

With respect to claim 28, Pekny discloses, in column 6, that the instructions to replace memory unit with the alternate memory unit comprises instructions to: cause the memory unit to be un-accessible at a memory address [defective cell]; and cause the alternate memory unit to be accessible at the memory address [redundant cell]. It

the cited section, Pekny indicated that "...access the redundant memory cells in response to address locations of defective primary cells locations..."

With respect to claim 31, Pekny discloses, in column 1, that the memory device is a flash memory block.

Remarks

7. Applicant's arguments filed August 29, 2005 and February 16, 2006 have been fully reconsidered but they are not persuasive.

Applicant's argument, filed August 29, 2005, argued that the Pekny reference does not disclose a memory device that in which "...detecting is performed during an erase operation..." Additionally, Applicant stated that the verify step is separate from the erase step. However, the Pekny reference does, in fact, state clearly that the detection of a defective memory cell is done during either a program or an erase operation – see column 2, lines 35-45. Further, Applicant's argument with regards to the verify step is separate step from the erase step. However, it is noted that the verify step is a part of the overall "erase operation" – see figure 4 and its support.

Additionally, Applicant's argument, filed February 16, 2006, stated that the Santin reference does not disclose how the redundancy circuits detect defective memory cells; thus, concluded that Santin does not teach a failure detection unit configured to monitor electrical characteristics in the plurality of accessible memory units. On the contrary, column 4, lines 45-65, discloses that a match circuit within the redundancy circuits generates a match signal that determines whether a memory cell is defective or not.

Therefore, it is reasonable to assume that the match signal is functioning as a comparator to compare certain characteristics of a memory cell to determine whether or not it's defective.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

Allowable Subject Matter

8. Claims 14-19 are allowable over the prior art of record.

9. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- The detecting the characteristic comprises: monitoring a resistance during an erase attempt; and identifying the defect when the resistance passes a predetermined resistance threshold.

- The causing the alternate memory unit to be accessible comprises: programming address status bits of the alternate memory unit with the memory address.
- The causing the alternate memory unit to be accessible comprises: setting a used status bit of the alternate memory unit.
- A failure detection unit coupled to the plurality of accessible memory units configured to monitor electrical characteristics in the plurality of accessible memory units during an erase operation and detect an electrical characteristic that identifies a defect in one of the plurality of accessible memory units; and a redundant block swap unit coupled to the plurality of accessible memory units and the one or more redundant memory units, the redundant block swap unit configured to replace the one of the plurality of accessible memory units with one of the one or more redundant memory units.
- The failure detection circuit comprising: a current detection unit to detect a current in one of the plurality of accessible memory units during an erase operation.
- The redundant block swap unit is configured to program the address status bits and the used status bit to cause the plurality of memory cells to be accessible.

Conclusion

10. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

12. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2827
April 10, 2006

MICHAEL TRAN
PRIMARY EXAMINER